Inter-channel Phase Errors In Free-Running Digital Converters

Availability of inexpensive DSP boards stimulated a design trend of incorporating such boards into multi-channel loudspeaker systems. Such design would often employ one DSP crossover per loudspeaker box. In a typical design, all digital converters within each board are clock-synchronized to a crystal oscillator, from which sampling frequency is derived.

In a multi-channel system, each DSP board runs with it's own local oscillator. Therefore, if multiple DSP boards are allowed to run without synchronization and time alignment, there is a possibility, that inter-channel phase errors will develop between loudspeakers. The magnitude of the phase error will depend on sampling frequency. To make things worse, the phase error will not be constant. It will fluctuate between 0 deg and an angle determined by the sampling frequency. The frequency of those fluctuations depends on the sample clock difference between the DSP board.

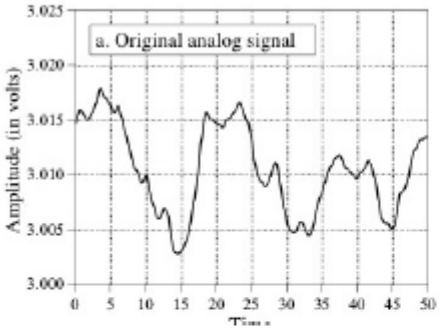
For instance, if DSP1 board runs with sample clock of 48000.1Hz and DSP2 board runs with sample clock of 48000.2Hz, there will be 0.1Hz fluctuating frequency of the phase error. 0.1Hz = 1 revolution per 10 seconds, so there will be a slowly small shifting of the image image between the front loudspeakers.

In order to understand the roots of the issue, please review a few simple issues related to digitizing signals. In order to make things simple, I assumed, that ADC is performed by standard "sample-and-hold" digital converter, and DAC is performed by standard "zero-order holder" digital converter. Also, processing time between ADC and DAC is zero, so whatever is digitized at the input – it will appear instantly at the output DAC.

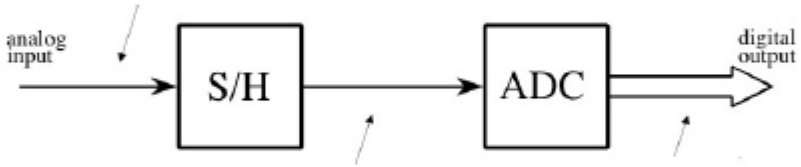
We should now review some digital basics.

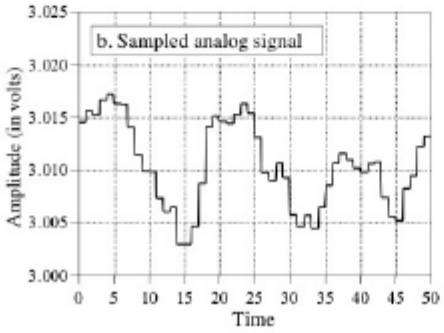
http://tintoretto.ucsd.edu/jorge/teaching/mae143a/lectures/8sampling.pdf

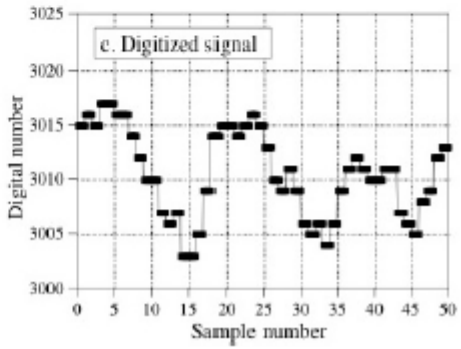
Illustration of digitization process



We will look into two stages of the ADC process: *sample and hold* and *quantization. After* that, the signal is *encoded* into bits.



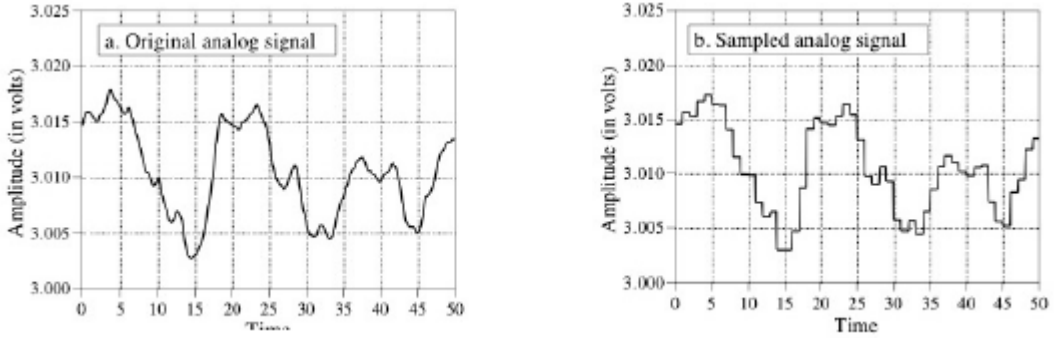




Digitization process

Sample and hold:

The output only changes at periodic instants of time. The independent variable now takes values in a discrete set

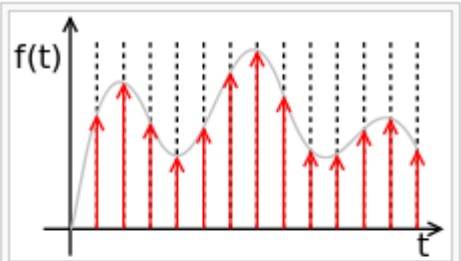


Sample and hold

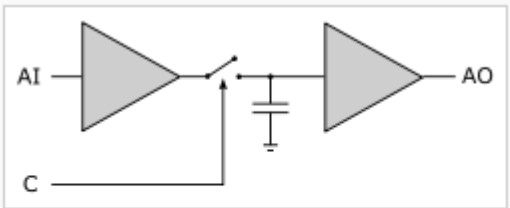
From Wikipedia, the free encyclopedia

For Neil Young song, see Trans (album). For remix album by Simian Mobile Disco, see Sample and Hold.

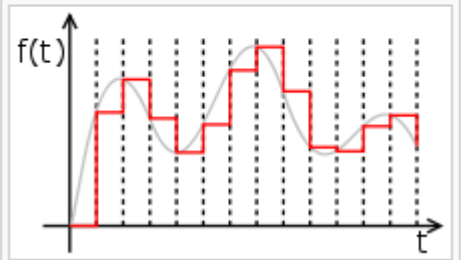
In electronics, a **sample and hold** (**S/H**, also "follow-and-hold"[1]) circuit is an analog device that samples (captures, grabs) the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimum period of time. Sample and hold circuits and related peak detectors are the elementary analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.[2]



Sample times.



A simplified sample and hold circuit diagram. AI is an analog input, AO — an analog output, C — a control signal.

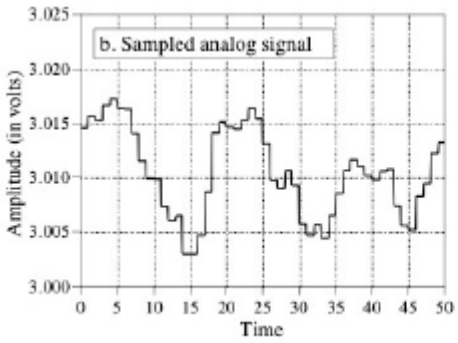


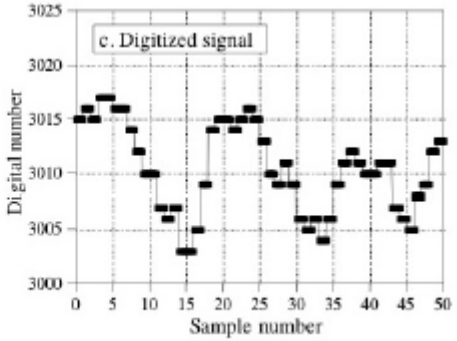
Sample and hold.

Digitization process

Quantization:

Each flat region in the sampled signal is "rounded-off" to the nearest member of a set of discrete values (e.g., nearest integer)





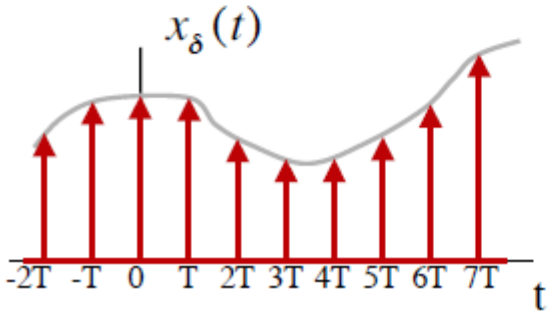
Digital-to-analog conversion

However, the ideal operation just described assumes availability of infinitely many samples - not realistic!

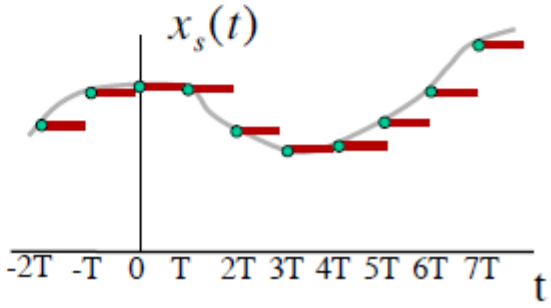
Practical operation uses only a finite number of samples. Many techniques can be used to approximately reconstruct the signal.

One such technique is a **zero-order holder**.

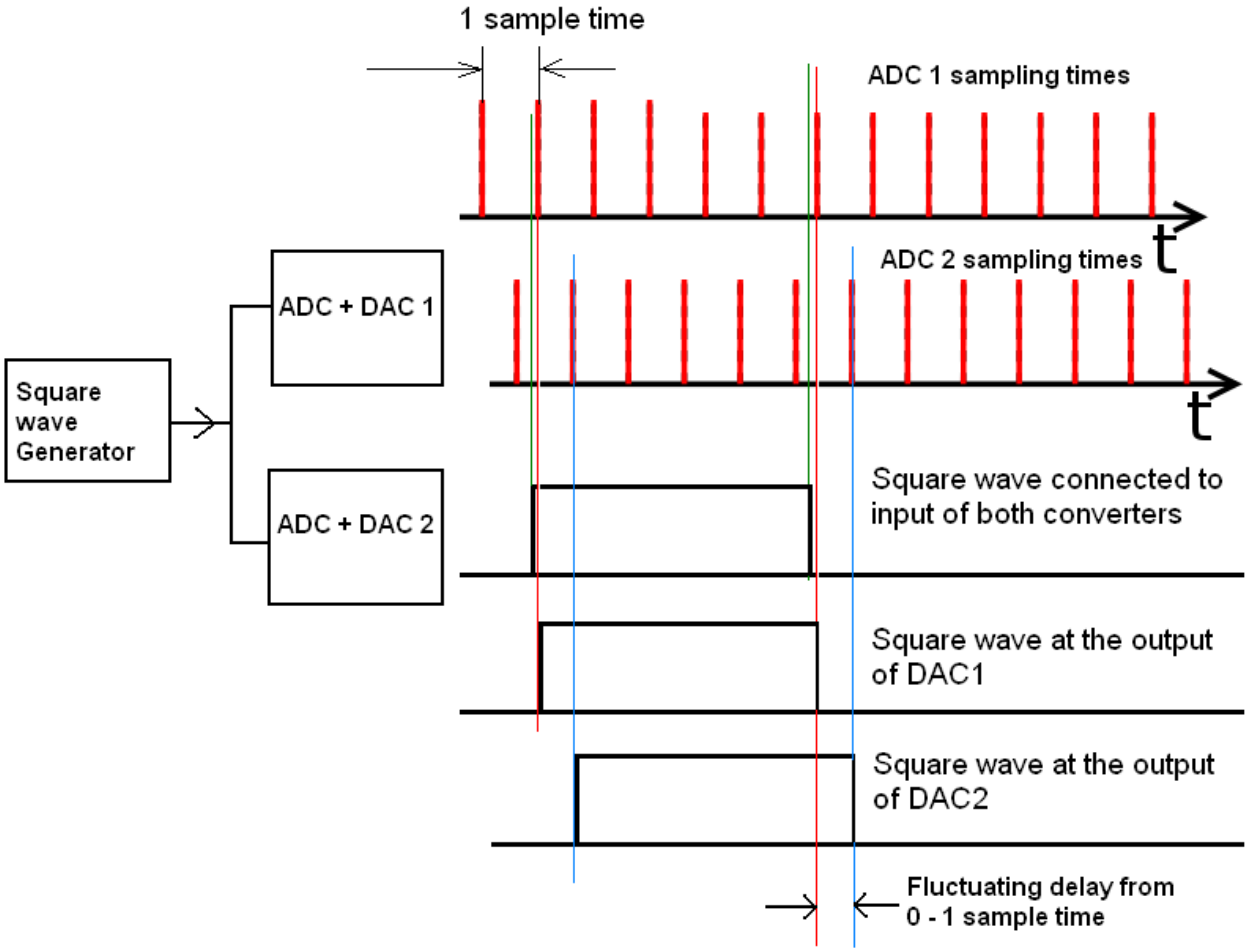
Modulated impulses



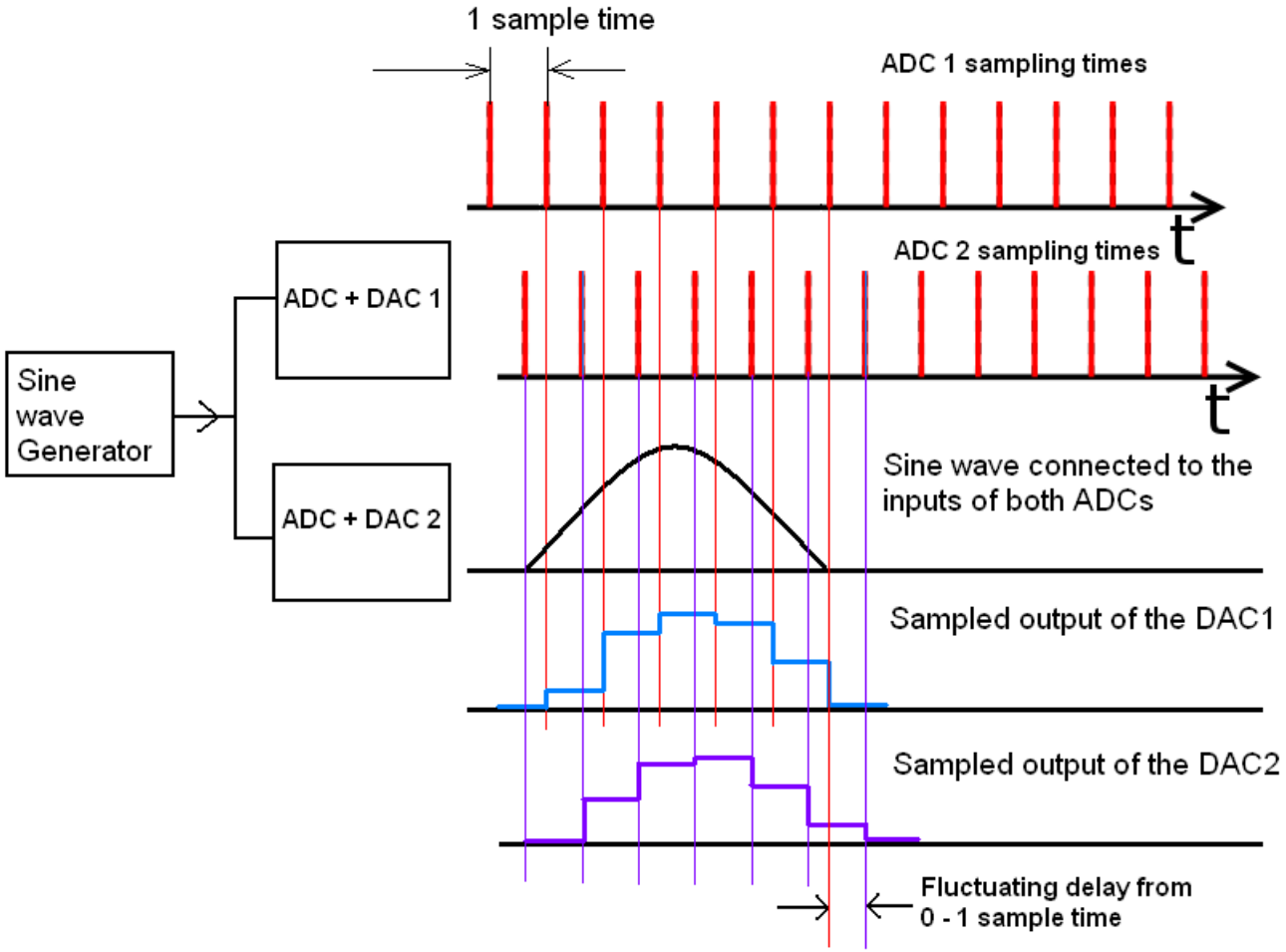
After Zero-Order Holder



In the following example, a square wave generator feeds two, “free running” DSP boards. Therefore **sampling time instances** are shifted between the boards, and ADC2 is lagging ADC1. It is observable, that square wave coming out of DAC2 will be time-shifted in reference to DAC1.



In the following example, a sine wave generator feeds two, “free running” DSP boards. Therefore **sampling time instances** are shifted between the boards, and ADC2 is lagging ADC1. It is observable, that sine wave coming out of DAC2 will be time-shifted in reference to DAC1.



The allowed time difference between stereo pair of loudspeaker is actually specified in AES document shown below.
http://www.aes.org/technical/documents/AESTD1001.pdf

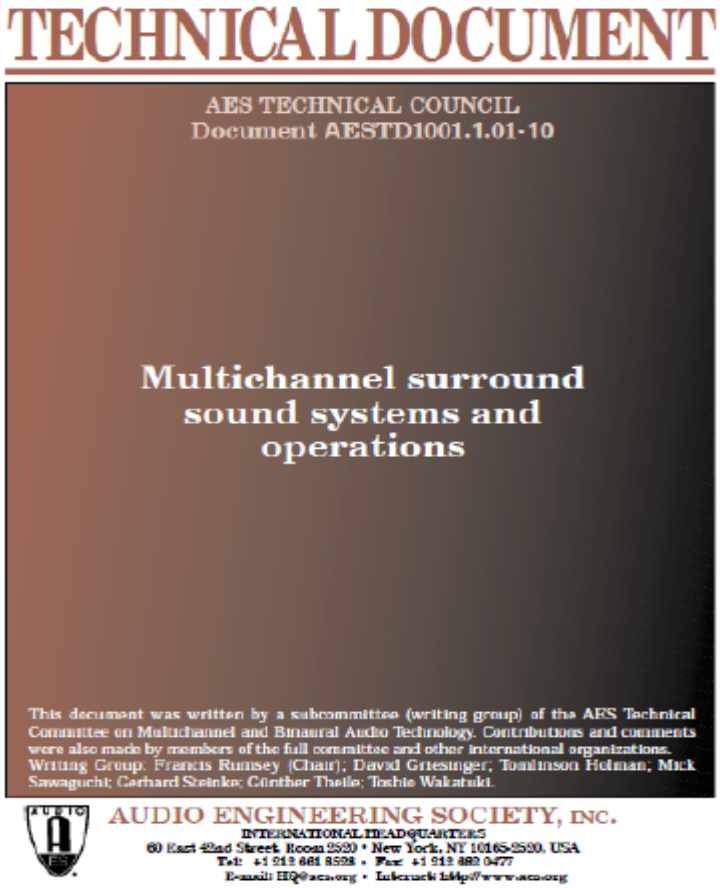


Table 3. Suggestions for reference monitor loudspeakers and advice for home loudspeakers.

Parameters	*Units/Conditions*	*Value*
Amplitude/frequency response Difference between front loudspeakers	40 Hz–16 kHz 0° ±10° Horizontal ±30° In the range >250 Hz to 2 kHz	 Tolerance 4 dB Deviation to 0°, 3 dB Deviation to 0°, 4 dB 0.5 dB
Directivity index	250 Hz–16 kHz	8 dB ±2 dB
Nonlinear distortion attenuation (SPL = 96 dB)	<100 Hz >100 Hz	–30 dB (=3%) –40 dB (=1%)
Transient fidelity Decay time t_s, for reduction to a level of 1/*e*, i.e., 0.37 of output level	t_s[s]	<5/*f* [Hz] (preferably 2.5/*f*)
Time delay Difference between stereo loudspeakers	∂t	≤10 µs
System dynamic range Maximum operating level (measurement acc. to IEC 60268, § 17.2, referred to 1 m distance)	$L_{\text{eff max}}$	>112 dB (at IEC 60268 program simulation noise or special condition)
Noise level	L_{noise}	≤10 dBA

Example below shows the recommended limit of phase difference between stereo loudspeakers (green curve) and the phase difference between two digital devices sampling at 48kHz, and differing by one sample of **20.38usec** (blue curve). It is observable in this example, that the "out-of-synch" condition alone, will result in failing of the AESTD1001.1.01-10 recommendations.

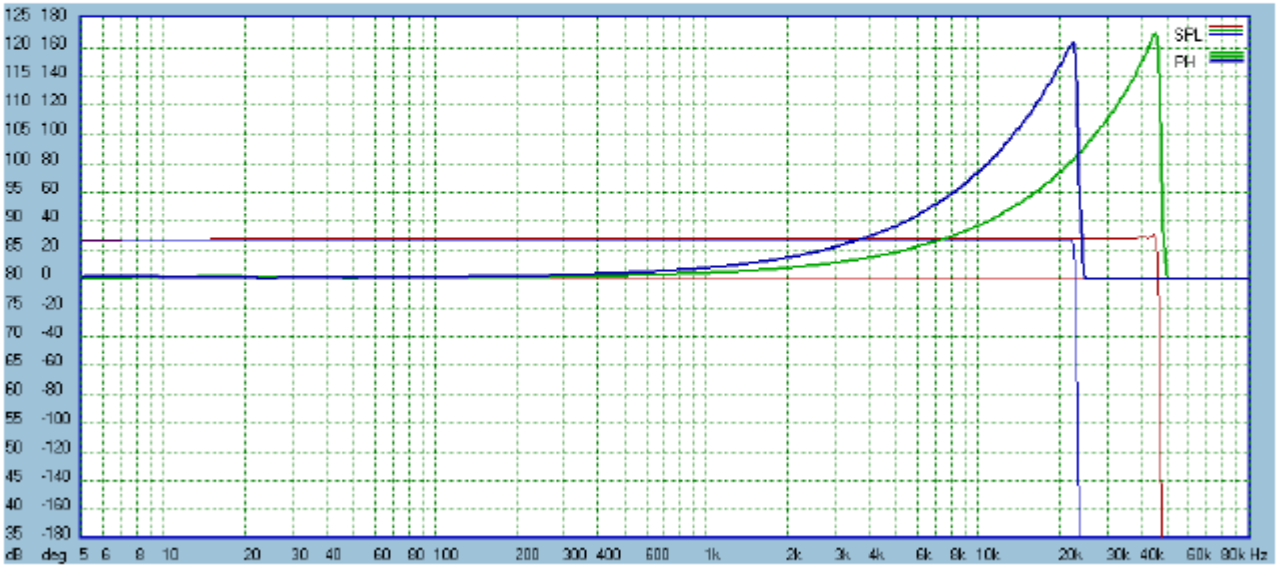


Figure 12. Sampling error (blue) of two ADC devices sampling with 48kHz.

If the sampling frequency is 96kHz, you would still be outside the 10usec recommendation. Setting sampling frequency to 192kHz would reduce the fluctuating phase error to about 5usec.

Obviously, the best option is to run all ADCs and DACs from single clock sourcve.